Attorney Docket: ET01-010

Reply to Office action of June 23,2004

## Amendments to the Drawings:

The attached sheets of drawings include changes to Figs. 1, 2, and 4a.

The first sheet, which includes Figs. 1-2, replaces the original sheet including

Figs. 1-2. In Figs 1-2, previously omitted parasitic capacitor Cp has been added.

The second sheet, which includes Figs. **4A-B**, replaces the original sheet including Figs. **4A-B**. In Fig. 4a, the element titled **C parasitic** has its titled shorted to **Cp** to conform with the element added to Figs. **1-2**.

#### **Attachment:**

**Annotated Sheets Showing Changes** 

Replacement Sheets

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Reply to Office action of June 23,2004

**REMARKS/ARGUMENTS** 

Examiner Nguyen is thanked for the thorough examination of the subject

Patent Application. The Claims have been carefully reviewed and amended, and

are considered to be in condition for allowance.

Reconsideration of the rejection under 35 USC §112, second paragraph,

of Claims 1-11 as being indefinite for failing to particularly point out and distinctly

claim the subject matter which the applicant regards as the invention is

requested in light of the following arguments. Claims 1-11 are amended to more

clearly define the "large capacitor" that is added between the bias node b1 and

the lower supply voltage **VSS**. The value of the large capacitor **CHC** is chosen

such that the capacitance coupling ration between the large capacitor and the

parasitic capacitor Cp between the bias node b1 and the lower supply voltage

VSS, is sufficiently large that the bias voltage VB11 is directly coupled to the

lower supply voltage **VSS**. The PMOS bias node is now the bias node **b1** and

appropriately defined.

Claims 3-9 are amended to depend on Claim 2. Claims 10 and 11 are

amended to define the coupling of the parasitic capacitor Cp between the bias

node **b1** and the lower supply voltage **VSS**.

Page 23 of 89

Reconsideration of the rejection under 35 USC §102(e) of Claims 1-11 as being anticipated by U.S. Patent 6,437,613 (Shim et al.) is requested in light of the following arguments.

Shim et al. does provide a first comparator **61** and second comparator **63** having a differential structure similar to the buffer input portion of this invention.

However, Shim et al. does not include

a large capacitor between the bias node and a lower supply voltage said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point; (Claim 1, Lines 4-10)

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a buffer output portion in communication with the buffer input portion for producing an output signal. (Claim 1, Lines 11-12)

The transistor **61a** is configured to be turned off and turned on according to the "voltage level of the first auxiliary signal VAUXL." The "voltage level of the first

Appl. No.: 10/631,84 Attorney Docket: ET01-010 Amdt. Dated: July 8, 2004 Reply to Office action of June 23,2004

comparison signal VCOML is prevented from being unstable." (Shim et al. Col. 6, Lines 27-33) The transistor **61a** is not configured as a large capacitor that provides a charge couple of the bias node **b1** to the lower supply voltage **VSS**.

Reconsideration of the objection to Claims 2 and 11 because of informalities is requested. The claims are amended to provide correct description of the elements and function of the elements.

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Reconsideration of the objection to the specification because of informalities on pages 4 and 5 is requested. The specification has been amended to incorporate the corrections requested by the examiner and to clarify the structure and function of the input buffer receiver of the invention.

Figs. 1, 2, and 4a have been modified with the changes marked in red on the attached drawings to. Approval of these changes is requested. No new matter has been added. Figs. 1 and 2 are modified to include the parasitic capacitor **Cp** present between the bias node and the lower supply voltage. The permits clarification of the description of the large capacitor **CHC** and it effects on the performance of the input buffer receiver of the invention.

Claims 12-42 are added to more completely claims the subject matter the applicant regards as the invention.

Attorney Docket: ET01-010
Reply to Office action of June 23,2004

The related art references made of record and not relied upon have been reviewed and it is agreed that they do not suggest the present detailed claimed invention.

Applicant respectfully requests that a timely Notice of Allowance for all claims be issued in this case.

It is requested that should Examiner Nguyen not find that the Claims are now allowable, that the undersigned be called at (845) 452-5863 to overcome any problems preventing allowance.

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Respectfully Submitted, George O. Saile & Associates

Billy J. Knowles, Reg. No. 42,752

Telephone: (845) 452-5863

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Attachments:

Attorney Docket: ET01-010

Reply to Office action of June 23,2004

## LOW JITTER INPUT BUFFER WITH SMALL INPUT SIGNAL SWING

#### **Background of the Invention**

Field of the Invention

[0001] The present invention generally relates to an interface circuit, and particularly to a low jitter input buffer.

Description of Related Art

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- [0002] Major design efforts have been directed at circuit design techniques involving input circuits for memory devices. A number of solutions have been proposed.
- [0003] U.S. Patent 5,978,310 (Bae et al) describes an input buffer for a DRAM memory device, which removes noise from the row address strobe. The device has a data output enable, which can be delayed for a predetermined time, and which also produces a contr o! signal for the output. There is also a buffer output for producing the noise free input according to the control signal.

Appl. No.: 10/631,84

Amdt. Dated: July 8, 2004

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Attorney Docket: ET01-010

Reply to Office action of June 23,2004

[0004] U.S. Patent 6,002,618 (Komarek et al) discloses an NMOS input receiver circuit for a read only memory. It includes a feedback loop to control hysteresis. There is a second stage and an additional output for the receiver. Switching noise from inside the memory is isolated and

cannot be fed back into the receiver circuit to affect the TTL voltage levels.

Wide, long FET sizes are used to minimize manufacture variations in the

receiver switching levels.

[0005] What is still needed is a mechanism by which an input buffer works in the presence of ground noise, specifically how capacitance can be used to reduce such noise for a memory input circuit.

#### Summary of the Invention

[0006] It is therefore an object of the present invention to provide an efficient circuit design technique for an input buffer receiver for a particular memory device[[,]] that works to filter ground noise. It is a further object of the invention to provide a means for reducing jitter in an input buffer. This is achieved by attaching a large capacitance to the PMOS-bias node of the input buffer receiver.

[0007] These and other objects are achieved by an input buffer receiver comprising: a buffer input portion for receiving an input signal SIGNAL\_IN; Amdt. Dated: July 8, 2004

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Reply to Office action of June 23,2004

a large capacitor capacitance CHC-between a PMOS-bias node and a VSS source lower supply voltage VSS, and a buffer output portion for producing an output signal SIGNAL\_OUT1. Furthermore, in the input buffer receiver, the VB11 gate biasing voltage of the bias node of transistors P11 and P12 is charge coupled to the VSS lower voltage source voltage. This results in a quicker response time for the output signal SIGNAL OUT1.

## **Brief Description of the Drawings**

- [8000] The foregoing and other objects, aspects, and advantages will be better understood from the following detailed description of a preferred 10 embodiment of the invention, with reference to the drawings, in which:
  - [0009] FIG. 1 is a diagram of an input buffer receiver according to the prior art.
- [0010] FIG. 2 is a diagram of an input buffer receiver according to the present invention. 15
  - [0011] FIGS.3A-B show the timing diagrams of the input buffer receiver of the present invention and the definitions of JITTER RISE and JITTER\_FALL.

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Attorney Docket: ET01-010

Reply to Office action of June 23,2004

[0012] FIGS. 4A-B illustrate the workings of capacitance capacitor CHC to reduce JITTER RISE and JITTER FALL.

#### **Detailed Description of the Invention**

- [0013] One embodiment of the present invention is provided below with reference to the accompanying diagrams.
- [0014] Referring to FIG. 1, the input buffer receiver of the prior art includes a buffer input portion 100 for receiving an input signal SIGNAL\_IN and a buffer output portion 200 for producing an output signal SIGNAL\_OUT.
- and N2, where a lower supply voltage VSS is applied to the source nodes of NMOS transistors N1 and N2, and PMOS transistors P1 and P2, where an upper voltage supply VDD is applied to the source nodes. The gate nodes of transistors P1 and P2 and the the drains of transistors N1 and P1 are connected together to form the biasing node b1. The biasing voltage VB1 is developed at the biasing node b1 as a result of the configuration of transistors P1 and P2. A parasitic capacitor Cp is present from the biasing node b1 to the ground reference node. and a signal VB1 is applied to the gate nodes of P1 and P2. In the prior art, a reference voltage VREF is applied to the gate of transistor N1, input signal SIGNAL IN is applied to

Attorney Docket: ET01-010
Reply to Office action of June 23,2004

the gate of <u>transistor N2</u>, and VB1 is applied to the drain of N1 and the drain of P1, as well as the PMOS bias node of P1 and P2. <u>Input signal</u> SIGNAL\_IN is a low swing signal coming from off chip. The buffer output portion 200 is comprised of a common node for the drain of <u>transistor N2</u> and drain of <u>transistor P2</u>, which serves as input to inverter I1. The output of inverter I1 is the output signal <u>output SIGNAL\_OUT</u>.

[0016] The ground noise (VSS noise), as described above, is developed between the lower supply voltage VSS and the ground reference voltage.

The magnitude of the VSS noise affects the delay timing from the input signal SIGNAL IN to the output signal SIGNAL OUT. The variation in the delay causes jitter in the rise and fall delays of the buffer and thus slower response times.

[0017] Referring to FIG. 2, the proposed invention is comprised of a similar buffer input portion 101 and a similar buffer output portion 201. The buffer input portion 101 is comprised of: NMOS transistors N11 and N12, where a the lower supply voltage VSS is applied to the source nodes of N11 and N12, and PMOS transistors P11 and P12, where an upper supply voltage VDD is applied to the source nodes. The gate nodes of transistors P11 and P12 and the the drains of transistors N11 and P11 are connected together to form the biasing node b11. The biasing voltage VB11 is

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Appl. No.: 10/631,84 Attorney Docket: ET01-010

Amdt. Dated: July 8, 2004 Reply to Office action of June 23,2004

developed at the biasing node b11 as a result of the configuration of transistors P11 and P12. A parasitic capacitor Cp is present from the biasing node b11 to the ground reference node. A signal VB11 is applied to the gate nodes of P11 and P12. A reference supply voltage VREF is applied to the gate of transistor N11, input signal SIGNAL\_IN is applied to the gate of N12, and VB11 is applied to the drain of N11 and the drain of P11. In the present invention, a large capacitance capacitor CHC is attached between the PMOS bias node VB11 b11 and the lower supply source voltage VSS. The buffer output portion 201 is comprised of a common node for the drain of transistor N12 and the drain of transistor P12, which serves as input to inverter I11. The output of inverter I11 is the output signal SIGNAL\_OUT1 of the invention.

[0018] The large capacitance CHC is in series with the parasitic <u>capacitor</u>

<u>Cp capacitance</u> of the input buffer receiver <u>devices-transistors</u> N11, P11,

and P12. The large capacitor CHC, as connected, is <u>designed to have an</u>

<u>extremely large capacitance relative to the parasitic capacitor Cp such that</u>

the bias voltage VB11 essentially follows the voltage changes in the lower supply voltage VSS preventing the effects of the VSS noise. This coupling ratio is determined by the formula:

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Attorney Docket: ET01-010
Reply to Office action of June 23,2004

where:

CHC is the capacitance value of the large capacitor

CHC.

<u>Cp is the capacitance value of the parasitic capacitor</u>
<u>Cp.</u>

[0019] Because of its large coupling ratio (very close to 1), the capacitor

CHC essentially charge couples the biasing voltage VB11 gate voltage of

the PMOS bias node b11, to the VSS source lower supply voltage VSS, of

devices N11 and N12. This forces the transistors N11 and N12 to activate

and deactivate essentially simultaneously, allowing for a quicker response
time on output signal SIGNAL\_OUT1.

[0020] FIGS. 3A-B are diagrams of timed operation showing the input signal SIGNAL\_IN, the source-lower supply voltage VSS, and the output signal SIGNAL\_OUT1 of the proposed invention. It should be noted that the input signal SIGNAL\_IN is defined as VIH=VREF+350mv and VIL=VREF-350mv, and VSS is 200mv. The output signal SIGNAL\_OUT1 is defined by the delayed signal-delay times\_DELTA1 or DELTA2, when input signal\_SIGNAL\_IN rises, and the delay times\_DELTA3 or DELTA4, when the input signal\_SIGNAL\_IN falls. The delay time\_DELTA1 is defined

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Attorney Docket: ET01-010
Reply to Office action of June 23,2004

as the delay from the rising edge of input signal SIGNAL. IN to the rising edge of output signal SIGNAL OUT, when VSS=200mv. It is the delay on output signal SIGNAL OUT1 when transistor N12 sees VSS noise and turns on weakly. The delay time DELTA2 is defined as the delay from the rising edge of input signal SIGNAL IN to the rising edge of output signal SIGNAL OUT1, when VSS=0v. It is the delay on of the output signal SIGNAL OUT1 when transistor N12 does not see VSS noise and turns on strongly. The delay time DELTA3 is defined as the delay from the falling edge of input signal SIGNAL IN to the falling edge of output SIGNAL OUT1, when VSS=0v. It is the delay on of the input signal SIGNAL\_OUT1 when transistor N12 does not see VSS noise and turns off weakly. DELTA4 is defined as the delay from the falling edge of input signal SIGNAL\_IN to the falling edge of output signal SIGNAL\_OUT1, when VSS=200mv. It is the delay seen on output signal SIGNAL OUT1 when transistor N12 sees VSS noise and turns off strongly. By definition. the delay times DELTA2 and DELTA4 are smaller than the delay times DELTA1 and DELTA3. The rise time jitter JITTER RISE is the difference between the delay times DELTA1 and DELTA2 when the input signal SIGNAL IN rises and the fall time jitter JITTER FALL is the difference between the delay times DELTA3 and DELTA4 when input signal SIGNAL IN falls. The intent of the invention capacitance large capacitor

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Attorney Docket: ET01-010
Reply to Office action of June 23,2004

CHC is to reduce <u>rise time jitter\_JITTER\_RISE</u> and <u>fall time jitter</u>

JITTER\_FALL by primarily having <u>devices\_transistors\_P12</u> and N12, activate, in the presence or absence of ground noise, almost simultaneously.

[0021] FIGS. 4A-B illustrate the workings of <u>large capacitor CHC. In Fig.</u>

4a, the large capacitor is shown in series with the parasitic capacitor Cp.

The <u>lts-large capacitance coupling ratio of the large capacitor CHC versus the capacitance of the parasitic capacitor Cp creates a charge coupling couples of the <u>PMOS</u>-bias node, <u>VB11\_b11</u>, of the input buffer receiver, to the <u>VSS source-lower supply</u> voltage <u>VSS</u>, of the input buffer receiver.

This results in a quicker response time for a input signal SIGNAL OUT1.</u>

[0022] While the invention has been described in terms of the preferred embodiments, those skilled in the art will recognize that various changes in form and details may be made without departing from the spirit and scope of the invention. The present invention covers modifications that fall within the range of the appended claims and their equivalents.

[0023] While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

Attorney Docket: ET01-010 Reply to Office action of June 23,2004

[0024] What is claimed is:

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Attorney Docket: ET01-010

Reply to Office action of June 23,2004

1. (Amended) An input buffer receiver comprising:

a buffer input portion for receiving an input signal-SIGNAL-IN, said 2 buffer input portion comprising a bias node; 3 a large capacitor capacitance between a PMOS the bias node and 4 a <del>VSS source lower supply voltage said large capacitor</del> 5 providing a coupling ratio between said large capacitor and a 6 parasitic capacitor coupled between said bias node and a 7 ground reference point approaching a unity value such that a 8 biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the 10 lower supply voltage and the ground reference point; and 11 a buffer output portion in communication with the buffer input 12 portion for producing an output signal-SIGNAL OUT1. 13

2. (Amended) The input buffer receiver of claim 1, wherein the buffer input portion which receives an the input signal SIGNAL IN further comprises:

a first transistor of a first conductivity type N11 having a source node to which a VSS source the lower supply voltage is applied, a gate node to which a reference voltage VREF is applied, and

Attorney Docket: ET01-010
Reply to Office action of June 23,2004

a drain node at which the biasing voltage is developed to which a signal VB11 is applied;

- a second transistor of a second conductivity type P11 having a drain node which is connected to the drain node of the first transistor N11, and a gate node at which the biasing voltage is developed to which a signal VB11 is applied, and a source node to which an upper supply voltage source VDD is applied;
- a third transistor of the second conductivity type P12 having a drain node which is connected to the drain of a fourth transistor-N12, a gate node at which the biasing voltage is developed to which a signal VB11 is applied, and a source node to which an the upper supply voltage source VDD is applied;
- a fourth transistor of the first conductivity type\_N12-having a source node to which a VSS source-lower suppply voltage is applied, a gate node to which an input signal SIGNAL\_IN is applied externally, and a drain node which is the an input to the buffer output portion.

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Attorney Docket: ET01-010
Reply to Office action of June 23,2004

 (Amended) The input buffer receiver of claim 2-1, wherein the first and fourth transistors, N11 and N12, are NMOS transistors, and the second and third transistors, P11 and P12, are PMOS transistors.

- 4. (Amended) The input buffer receiver of claim 2-1, wherein the large <u>capacitor eapacitance</u> is connected between the sources of the first and fourth transistors, N11 and N12, of the buffer input portion and the gate of the second transistor P11 of the buffer input portion.
- 5. (Amended) The input buffer receiver of claim 2-1, wherein the gate of the second transistor P11-is connected to its drain.
- (Amended) The input buffer receiver of claim 2-1, wherein the gate of the second transistor P11-is connected to the drain of the first transistor N11.
- 7. (Amended) The input buffer receiver of claim 2-1, wherein the gate of the second transistor P11-is connected to the gate of the third transistor P12.
- 8. (Amended) The input buffer receiver of claim\_2\_1, wherein the buffer output portion which produces an-output signal SIGNAL\_OUT1-comprises: a first inverter I11-connected to the drain of the third transistor P12-and the drain of the fourth transistor-N12;

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Attorney Docket: ET01-010
Reply to Office action of June 23,2004

9. (Amended) The input buffer receiver of claim 2-1, wherein P12 and N12

the third transistor and the fourth transistor activate almost simultaneously
to provide an efficient circuit design technique for filtering-minimize the

effects of ground noise on a delay jitter factor of said input buffer.

10. (Amended) The input buffer receiver of claim 1, involving a large capacitance coupling ratio, which wherein the large capacitor charge couples the PMOS bias node of the input buffer receiver to the VSS source lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{\text{CHC}}{\text{Cp + CHC}} \approx 1$$

where:

CHC is the capacitance value of the large capacitor, and

**Cp** is the capacitance value of the parasitic capacitor.

11. (Amended) The input buffer receiver of claim 1, involving a wherein the capacitance value of the large capacitor relative to said parasitic capacitor

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Attorney Docket: ET01-010
Reply to Office action of June 23,2004

capacitance coupling ratio, which results in a quicker response time for the 3 output signal a SIGNAL OUT1. 4 12. (New) An integrated circuit formed on a substrate comprising: an input buffer receiver for receiving an input signal and connected 2 3 to said distribution network, said input buffer comprising: a buffer input portion for receiving the input signal, said 4 buffer input portion comprising a bias node; 5 a large capacitor between the bias node and a lower 6 supply voltage, said large capacitor providing a 7 coupling ratio between said large capacitor and a 8 9 parasitic capacitor coupled between said bias node 10 and a ground reference point approaching a unity 11 value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects 12 of a ground noise signal between the lower supply 13 voltage and the ground reference point; and 14

a buffer output portion in communication with the buffer

input portion for producing an output signal.

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Attorney Docket: ET01-010

Reply to Office action of June 23,2004

1 13. (New) The integrated circuit of claim 12, wherein the buffer input portion of the input buffer receiver further comprises:

- a first transistor of a first conductivity type having a source node to which the lower supply voltage is applied, a gate node to which a reference voltage is applied, and a drain node at which the biasing voltage is developed;
- a second transistor of a second conductivity type having a drain node which is connected to the drain node of the first transistor, and a gate node at which the biasing voltage is developed, and a source node to which an upper supply voltage source is applied;
- a third transistor of the second conductivity type having a drain node which is connected to the drain of a fourth transistor, a gate node at which the biasing voltage is developed, and a source node to which the upper supply voltage source is applied;
- a fourth transistor of the first conductivity type having a source node to which lower supply voltage is applied, a gate node to which

Attorney Docket: ET01-010
Reply to Office action of June 23,2004

an input signal is applied externally, and a drain node which is an input to the buffer output portion.

- 1 14. (New) The integrated circuit of claim 13, wherein the first and fourth
  2 transistors are NMOS transistors, and the second and third transistors are
  3 PMOS transistors.
- 1 15. (New) The integrated circuit of claim 13, wherein the large capacitor is
  2 connected between the sources of the first and fourth transistorsof the
  3 buffer input portion and the gate of the second transistor of the buffer input
  4 portion.
- 1 16. (New) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to its drain.
- 1 17. (New) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to the drain of the first transistor.
- 1 18. (New) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to the gate of the third transistor.
- 19. (New) The integrated circuit of claim 13, wherein the buffer output portion
  which produces output signal comprises: a first inverter connected to the
  drain of the third transistor and the drain of the fourth transistor;

Attorney Docket: ET01-010

Reply to Office action of June 23,2004

1 20. (New) The integrated circuit of claim 13, wherein the third transistor and
2 the fourth transistor activate almost simultaneously to minimize the effects
3 of ground noise on a delay jitter factor of said input buffer.

1 21. (New) The integrated circuit of claim 12, wherein the large capacitor
2 charge couples the bias node of the input buffer receiver to the lower
3 supply voltage of the input buffer receiver and wherein a capacitance
4 value of the large capacitor is selected by the formula:

$$\frac{\text{CHC}}{\text{Cp+CHC}} \approx 1$$

6 where:

7 **CHC** is the capacitance value of the large capacitor,

8 and

9 **Cp** is the capacitance value of the parasitic capacitor.

- 1 22. (New) The integrated circuit of claim 12, wherein the capacitance value of
  2 the large capacitor relative to said parasitic capacitor results in a quicker
  3 response time for the output signal.
- 1 23. (New) A method for minimizing effects of ground noise on an input buffer receiver comprising the steps of:

Attorney Docket: ET01-010 Reply to Office action of June 23,2004

3		forming a buffer input portion for receiving an input signal on a
4		substrate;
5		forming a bias node within said buffer input portion;
6		connecting said a lower supply voltage to said buffer input portion;
7		forming a large capacitor between the bias node and the lower
8		supply voltage said large capacitor providing a coupling ratio
9		between said large capacitor and a parasitic capacitor coupled
10		between said bias node and a ground reference point
11		approaching a unity value such that a biasing voltage at said
12		biasing node follows said lower supply voltage to minimize
13		effects of a ground noise signal between the lower supply
14		voltage and the ground reference point; and
15		forming a buffer output portion on said substrate in communication
16		with the buffer input portion for producing an output signal.
1	24.	(New) The method of claim 23, wherein forming the buffer input portion
2		further comprises the steps of:
3		forming a first transistor of a first conductivity type on said
4		substrate;

applying the lower supply voltage to a source node of the first 5 transistor; 6 applying a reference voltage to a gate node of the first transistor; 7 connecting a drain node of the first transistor to develop as biasing 8 voltage at said drain node; 10 forming a second transistor of a second conductivity type on said substrate; 11 connecting a drain node of the second transistor to the drain node 12 of the first transistor: 13 connecting a gate node of the second transistor to the drain node of 14 the first transistor for developing the biasing voltage; and 15 connecting a source node of the second transistor to an upper 16 17 supply voltage; forming a third transistor of the second conductivity type on said 18 substrate: 19 connecting a drain node of the third transistor to the drain of a 20 fourth transistor; 21

connecting a gate node of the third transistor to the drain node of 22 the first transistor for developing the biasing voltage; 23 connecting a source node of the third transistor to the upper supply 24 voltage source; 25 forming a fourth transistor of the first conductivity type on said 26 substrate; 27 connecting a source node of the fourth transistor to the lower 28 supply voltage; 29 30 connecting a gate node of the fourth transistor to receive an input signal externally; and 31 32 connecting a drain node of the fourth transistor to an input to the buffer output portion. 33 25. (New) The method of claim 24, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS 2 transistors. 3 26. (New) The method of claim 24, wherein forming the large capacitor comprises the step of: 2

Attorney Docket: ET01-010

Reply to Office action of June 23,2004

connecting said large capacitor between the sources of the first and 3 fourth transistors of the buffer input portion and the gate of the second transistor of the buffer input portion. 5 27. (New) The method of claim 24, wherein forming the buffer input portion further comprises the steps of: 2 connecting the gate of the second transistor to its drain. 3 28. (New) The method of claim 24, wherein forming the buffer input portion further comprises the steps of: 2 connecting the gate of the second transistor to the gate of the third 3 transistor. 29. (New) The method of claim 24, wherein forming the buffer output portion which produces output signal comprises the step of: 2 3 forming a first inverter on said substrate; and connecting an input of said first inverter to the drain of the third 4 transistor and the drain of the fourth transistor; 5

Attorney Docket: ET01-010

Reply to Office action of June 23,2004

1 30. (New) The method of claim 24, wherein the third transistor and the fourth
2 transistor activate almost simultaneously to minimize the effects of ground
3 noise on a delay jitter factor of said input buffer.

1 31. (New) The method of claim 23, wherein the large capacitor charge
2 couples the bias node of the input buffer receiver to the lower supply
3 voltage of the input buffer receiver and wherein a capacitance value of the
4 large capacitor is selected by the formula:

$$\frac{\text{CHC}}{\text{Cp+CHC}} \approx 1$$

6 where:

7 CHC is the capacitance value of the large capacitor,

8 and

9 **Cp** is the capacitance value of the parasitic capacitor.

- 1 32. (New) The method of claim 23, wherein the capacitance value of the large
  2 capacitor relative to said parasitic capacitor results in a quicker response
  3 time for the output signal.
- 1 33. (New) An apparatus for minimizing effects of ground noise on an input buffer receiver comprising:

Attorney Docket: ET01-010
Reply to Office action of June 23,2004

3 means for forming a buffer input portion for receiving an input signal 4 on a substrate; means for forming a bias node within said buffer input portion; 5 means for connecting said a lower supply voltage to said buffer 6 input portion; means for forming a large capacitor between the bias node and the 8 lower supply voltage said large capacitor providing a coupling 9 10 ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point 11 12 approaching a unity value such that a biasing voltage at said 13 biasing node follows said lower supply voltage to minimize 14 effects of a ground noise signal between the lower supply 15 voltage and the ground reference point; and means for forming a buffer output portion on said substrate in 16 communication with the buffer input portion for producing an 17 output signal. 18 34. (New) The apparatus of claim 23, wherein forming the buffer input portion further comprises: 2

Attorney Docket: ET01-010 Reply to Office action of June 23,2004

3	means for forming a first transistor of a first conductivity type on
4	said substrate;
5	means for applying the lower supply voltage to a source node of the
6	first transistor;
7	means for applying a reference voltage to a gate node of the first
8	transistor;
9	means for connecting a drain node of the first transistor to develop
0	as biasing voltage at said drain node;
11	means for forming a second transistor of a second conductivity type
12	on said substrate;
13	means for connecting a drain node of the second transistor to the
14	drain node of the first transistor;
15	means for connecting a gate node of the second transistor to the
16	drain node of the first transistor for developing the biasing
17	voltage; and
18	means for connecting a source node of the second transistor to an
19	upper supply voltage;

20	means for forming a third transistor of the second conductivity type
. 21	on said substrate;
22	means for connecting a drain node of the third transistor to the
23	drain of a fourth transistor;
24	means for connecting a gate node of the third transistor to the drain
25	node of the first transistor for developing the biasing voltage;
26	means for connecting a source node of the third transistor to the
27	upper supply voltage source;
28	means for forming a fourth transistor of the first conductivity type on
29	said substrate;
30	means for connecting a source node of the fourth transistor to the
31	lower supply voltage;
32	means for connecting a gate node of the fourth transistor to receive
33	an input signal externally; and
34	connecting a drain node of the fourth transistor to an input to the
35	buffer output portion.

Attorney Docket: ET01-010

Reply to Office action of June 23,2004

- 1 35. (New) The apparatus of claim 24, wherein the first and fourth transistors
  2 are NMOS transistors, and the second and third transistors are PMOS
  3 transistors.
- 1 36. (New) The apparatus of claim 24, wherein means for forming the large capacitor comprises:
- means for connecting said large capacitor between the sources of
  the first and fourth transistors of the buffer input portion and the
  gate of the second transistor of the buffer input portion.
- 1 37. (New) The apparatus of claim 24, wherein means for forming the buffer input portion further comprises:
- means for connecting the gate of the second transistor to its drain.
- 1 38. (New) The apparatus of claim 24, wherein means for forming the buffer input portion further comprises the steps of:
- means for connecting the gate of the second transistor to the gate

  of the third transistor.
- 1 39. (New) The apparatus of claim 24, wherein means for forming the buffer output portion which produces output signal comprises:

means for forming a first inverter on said substrate; and
means for connecting an input of said first inverter to the drain of
the third transistor and the drain of the fourth transistor;

- 1 40. (New) The apparatus of claim 24, wherein the third transistor and the
  2 fourth transistor activate almost simultaneously to minimize the effects of
  3 ground noise on a delay jitter factor of said input buffer.
- 1 41. (New) The apparatus of claim 23, wherein the large capacitor charge
  2 couples the bias node of the input buffer receiver to the lower supply
  3 voltage of the input buffer receiver and wherein a capacitance value of the
  4 large capacitor is selected by the formula:

$$\frac{\text{CHC}}{\text{Cp+CHC}} \approx 1$$

6 where:

7 CHC is the capacitance value of the large capacitor

CHC, and

9 **Cp** is the capacitance value of the parasitic capacitor

10 Cp.

Appl. No.: 10/631,84 Attorney Docket: ET01-010 Reply to Office action of June 23,2004

1 42. (New) The apparatus of claim 23, wherein the capacitance value of the
2 large capacitor relative to said parasitic capacitor results in a quicker

response time for the output signal.

#### **Abstract**

[0025] A particular input buffer receiver includes a buffer input portion for receiving an input signal-SIGNAL\_IN, a large <u>capacitor capacitance CHC</u> between the PMOS-a bias node and the <del>VSS source-lower supply voltage, and a buffer output portion for producing an output signal-SIGNAL\_OUT1.</del>

The circuit works to remove ground noise by charge coupling the <del>VB11</del> bias voltage <u>developed at the bias node</u> to the <del>VSS source-lower supply voltage of the input device.</del>

#### Clean Copy of Specification showing changes

# LOW JITTER INPUT BUFFER WITH SMALL INPUT SIGNAL SWING

#### **Background of the Invention**

5 Field of the Invention

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[0001] The present invention generally relates to an interface circuit, and particularly to a low jitter input buffer.

#### Description of Related Art

- [0002] Major design efforts have been directed at circuit design techniques involving input circuits for memory devices. A number of solutions have been proposed.
- [0003] U.S. Patent 5,978,310 (Bae et al) describes an input buffer for a DRAM memory device, which removes noise from the row address strobe. The device has a data output enable, which can be delayed for a predetermined time, and which also produces a control signal for the output. There is also a buffer output for producing the noise free input according to the control signal.

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[0004] U.S. Patent 6,002,618 (Komarek et al) discloses an NMOS input receiver circuit for a read only memory. It includes a feedback loop to control hysteresis. There is a second stage and an additional output for the receiver. Switching noise from inside the memory is isolated and cannot be fed back into the receiver circuit to affect the TTL voltage levels. Wide, long FET sizes are used to minimize manufacture variations in the receiver switching levels.

[0005] What is still needed is a mechanism by which an input buffer works in the presence of ground noise, specifically how capacitance can be used to reduce such noise for a memory input circuit.

### **Summary of the Invention**

- [0006] It is therefore an object of the present invention to provide an efficient circuit design technique for an input buffer receiver for a particular memory device that works to filter ground noise. It is a further object of the invention to provide a means for reducing jitter in an input buffer. This is achieved by attaching a large capacitance to the bias node of the input buffer receiver.
- [0007] These and other objects are achieved by an input buffer receiver comprising: a buffer input portion for receiving an input signal; a large capacitor between a bias node and a lower supply voltage VSS, and a

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buffer output portion for producing an output signal. Furthermore, in the input buffer receiver, the biasing voltage of the bias node is charge coupled to the lower voltage source. This results in a quicker response time for the output signal.

## **Brief Description of the Drawings**

- [0008] The foregoing and other objects, aspects, and advantages will be better understood from the following detailed description of a preferred embodiment of the invention, with reference to the drawings, in which:
- [0009] FIG. 1 is a diagram of an input buffer receiver according to the prior art.
  - [0010] FIG. 2 is a diagram of an input buffer receiver according to the present invention.
- [0011] FIGS.3A-B show the timing diagrams of the input buffer receiver of the present invention and the definitions of JITTER\_RISE and

  JITTER\_FALL.
  - [0012] FIGS. 4A-B illustrate the workings of capacitor CHC to reduce

    JITTER RISE and JITTER FALL.

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### **Detailed Description of the Invention**

[0013] One embodiment of the present invention is provided below with reference to the accompanying diagrams.

[0014] Referring to FIG. 1, the input buffer receiver of the prior art includes a buffer input portion 100 for receiving an input signal SIGNAL\_IN and a buffer output portion 200 for producing an output signal SIGNAL\_OUT.

and N2, where a lower supply voltage VSS is applied to the source nodes of NMOS transistors N1 and N2, and PMOS transistors P1 and P2, where an upper voltage supply VDD is applied to the source nodes. The gate nodes of transistors P1 and P2 and the the drains of transistors N1 and P1 are connected together to form the biasing node b1. The biasing voltage VB1 is developed at the biasing node b1 as a result of the configuration of transistors P1 and P2. A parasitic capacitor Cp is present from the biasing node b1 to the ground reference node. In the prior art, a reference voltage VREF is applied to the gate of transistor N1, input signal SIGNAL\_IN is applied to the gate of transistor N2. Input signal SIGNAL\_IN is a low swing signal coming from off chip. The buffer output portion 200 is comprised of a common node for the drain of transistor N2 and drain of transistor P2,

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which serves as input to inverter I1. The output of inverter I1 is the output signal output SIGNAL OUT.

[0016] The ground noise (VSS noise), as described above, is developed between the lower supply voltage VSS and the ground reference voltage. The magnitude of the VSS noise affects the delay timing from the input signal SIGNAL\_IN to the output signal SIGNAL\_OUT. The variation in the delay causes jitter in the rise and fall delays of the buffer and thus slower response times.

[0017] Referring to FIG. 2, the proposed invention is comprised of a similar buffer input portion 101 and a similar buffer output portion 201. The buffer input portion 101 is comprised of: NMOS transistors N11 and N12, where the lower supply voltage VSS is applied to the source nodes of N11 and N12, and PMOS transistors P11 and P12, where an upper supply voltage VDD is applied to the source nodes. The gate nodes of transistors P11 and P12 and the the drains of transistors N11 and P11 are connected together to form the biasing node b11. The biasing voltage VB11 is developed at the biasing node b11 as a result of the configuration of transistors P11 and P12. A parasitic capacitor Cp is present from the biasing node b11 to the ground reference node. A reference supply voltage VREF is applied to the gate of transistor N11, input signal SIGNAL\_IN is applied to the gate of N12. In the present invention, a large

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capacitor CHC is attached between the bias node b11 and the lower supply voltage VSS. The buffer output portion 201 is comprised of a common node for the drain of transistor N12 and the drain of transistor P12, which serves as input to inverter I11. The output of inverter I11 is the output signal SIGNAL OUT1 of the invention.

[0018] The large capacitance CHC is in series with the parasitic capacitor Cp of the input buffer receiver transistors N11, P11, and P12. The large capacitor CHC, as connected, is designed to have an extremely large capacitance relative to the parasitic capacitor Cp such that the bias voltage VB11 essentially follows the voltage changes in the lower supply voltage VSS preventing the effects of the VSS noise. This coupling ratio is determined by the formula:

$$\frac{\text{CHC}}{\text{Cp} + \text{CHC}} \approx 1$$

where:

CHC is the capacitance value of the large capacitor CHC.

Cp is the capacitance value of the parasitic capacitor Cp.

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- [0019] Because of its large coupling ratio (very close to 1), the capacitor CHC essentially charge couples the biasing voltage VB11 bias node b11, to the lower supply voltage VSS, of devices N11 and N12. This forces the transistors N11 and N12 to activate and deactivate essentially simultaneously, allowing for a quicker response time on output signal SIGNAL OUT1.
- FIGS. 3A-B are diagrams of timed operation showing the input [0020] signal SIGNAL IN, the lower supply voltage VSS, and the output signal SIGNAL OUT1 of the proposed invention. It should be noted that the input signal SIGNAL IN is defined as VIH=VREF+350mv and VIL=VREF-10 350mv, and VSS is 200mv. The output signal SIGNAL OUT1 is defined by the delay times DELTA1 or DELTA2, when input signal SIGNAL IN rises, and the delay times DELTA3 or DELTA4, when the input signal SIGNAL IN falls. The delay time DELTA1 is defined as the delay from the rising edge of input signal SIGNAL IN to the rising edge of output signal 15 SIGNAL OUT, when VSS=200mv. It is the delay on output signal SIGNAL OUT1 when transistor N12 sees VSS noise and turns on weakly. The delay time DELTA2 is defined as the delay from the rising edge of input signal SIGNAL IN to the rising edge of output signal SIGNAL\_OUT1, when VSS=0v. It is the delay of the output signal 20 SIGNAL OUT1 when transistor N12 does not see VSS noise and turns on

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strongly. The delay time DELTA3 is defined as the delay from the falling edge of input signal SIGNAL IN to the falling edge of output SIGNAL OUT1, when VSS=0v. It is the delay of the input signal SIGNAL OUT1 when transistor N12 does not see VSS noise and turns off weakly. DELTA4 is defined as the delay from the falling edge of input signal SIGNAL\_IN to the falling edge of output signal SIGNAL\_OUT1, when VSS=200mv. It is the delay seen on output signal SIGNAL OUT1 when transistor N12 sees VSS noise and turns off strongly. By definition, the delay times DELTA2 and DELTA4 are smaller than the delay times DELTA1 and DELTA3. The rise time jitter JITTER\_RISE is the difference between the delay times DELTA1 and DELTA2 when the input signal SIGNAL IN rises and the fall time jitter JITTER FALL is the difference between the delay times DELTA3 and DELTA4 when input signal SIGNAL\_IN falls. The intent of the invention large capacitor CHC is to reduce rise time jitter JITTER RISE and fall time jitter JITTER FALL by primarily having transistors P12 and N12, activate, in the presence or absence of ground noise, almost simultaneously.

[0021] FIGS. 4A-B illustrate the workings of large capacitor CHC. In Fig.

4a, the large capacitor is shown in series with the parasitic capacitor Cp.

The large capacitance coupling ratio of the large capacitor CHC versus the capacitance of the parasitic capacitor Cp creates a charge coupling of

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the bias node, b11, of the input buffer receiver, to the lower supply voltage VSS, of the input buffer receiver. This results in a quicker response time for a input signal SIGNAL OUT1.

[0022] While the invention has been described in terms of the preferred embodiments, those skilled in the art will recognize that various changes in form and details may be made without departing from the spirit and scope of the invention. The present invention covers modifications that fall within the range of the appended claims and their equivalents.

[0023] While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

[0024] What is claimed is:

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1	1.	(Amended) An input buffer receiver comprising:
2		a buffer input portion for receiving an input signal, said buffer input portion comprising a bias node;
4		a large capacitor between the bias node and a lower supply voltage
5		said large capacitor providing a coupling ratio between said
6		large capacitor and a parasitic capacitor coupled between said
7		bias node and a ground reference point approaching a unity
8		value such that a biasing voltage at said biasing node follows
9		said lower supply voltage to minimize effects of a ground noise
10		signal between the lower supply voltage and the ground
11		reference point; and
12 13		a buffer output portion in communication with the buffer input portion for producing an output signal.
1	2.	(Amended) The input buffer receiver of claim 1, wherein the buffer input
2		portion which receives the input signal further comprises:
3		a first transistor of a first conductivity type having a source node to
4		which the lower supply voltage is applied, a gate node to which

biasing voltage is developed;

a reference voltage is applied, and a drain node at which the

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7	a second transistor of a second conductivity type having a drain
8	node which is connected to the drain node of the first transistor,
9	and a gate node at which the biasing voltage is developed, and
10	a source node to which an upper supply voltage source is
11	applied;

- a third transistor of the second conductivity type having a drain node which is connected to the drain of a fourth transistor, a gate node at which the biasing voltage is developed, and a source node to which the upper supply voltage source is applied;
- a fourth transistor of the first conductivity type having a source node to which lower suppply voltage is applied, a gate node to which an input signal is applied externally, and a drain node which is an input to the buffer output portion.
- 1 3. (Amended) The input buffer receiver of claim 2, wherein the first and
  2 fourth transistors are NMOS transistors, and the second and third
  3 transistors are PMOS transistors.
- 4. (Amended) The input buffer receiver of claim 2, wherein the large capacitor is connected between the sources of the first and fourth

- transistors of the buffer input portion and the gate of the second transistor of the buffer input portion.
- 1 5. (Amended) The input buffer receiver of claim 2, wherein the gate of the second transistor is connected to its drain.
- 1 6. (Amended) The input buffer receiver of claim 2, wherein the gate of the second transistor is connected to the drain of the first transistor.
- 7. (Amended) The input buffer receiver of claim 2, wherein the gate of the second transistor is connected to the gate of the third transistor.
- 1 8. (Amended) The input buffer receiver of claim 2, wherein the buffer output
  2 portion which produces output signal comprises: a first inverter connected
  3 to the drain of the third transistor and the drain of the fourth transistor;
- 9. (Amended) The input buffer receiver of claim 2, wherein the third transistor and the fourth transistor activate almost simultaneously to minimize the effects of ground noise on a delay jitter factor of said input buffer.
- 1 10. (Amended) The input buffer receiver of claim 1, wherein the large
  2 capacitor charge couples the bias node of the input buffer receiver to the
  3 lower supply voltage of the input buffer receiver and wherein a
  4 capacitance value of the large capacitor is selected by the formula:

5		Cp+CHC ≈ 1
6		where:
7		CHC is the capacitance value of the large capacitor,
8		and .
9		Cp is the capacitance value of the parasitic capacitor.
1	11.	(Amended) The input buffer receiver of claim 1, wherein the capacitance
2		value of the large capacitor relative to said parasitic capacitor results in a
3		quicker response time for the output signal.
1	12.	(New) An integrated circuit formed on a substrate comprising:
2		an input buffer receiver for receiving an input signal and connected
3		to said distribution network, said input buffer comprising:
4		a buffer input portion for receiving the input signal, said
5		buffer input portion comprising a bias node;
6		a large capacitor between the bias node and a lower
7		supply voltage, said large capacitor providing a
8		coupling ratio between said large capacitor and a
9		parasitic capacitor coupled between said bias node

10		and a ground reference point approaching a unity
11		value such that a biasing voltage at said biasing node
12		follows said lower supply voltage to minimize effects
13		of a ground noise signal between the lower supply
14		voltage and the ground reference point; and
15		a buffer output portion in communication with the buffer
16		input portion for producing an output signal.
1	13.	(New) The integrated circuit of claim 12, wherein the buffer input portion of
2		the input buffer receiver further comprises:
3		a first transistor of a first conductivity type having a source node to
4		which the lower supply voltage is applied, a gate node to which
5		a reference voltage is applied, and a drain node at which the
6		biasing voltage is developed;
7		a second transistor of a second conductivity type having a drain
8		node which is connected to the drain node of the first transistor,
9		and a gate node at which the biasing voltage is developed, and
10		a source node to which an upper supply voltage source is
11		applied;

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12	a third transistor of the second conductivity type having a drain
13	node which is connected to the drain of a fourth transistor, a
14	gate node at which the biasing voltage is developed, and a
15	source node to which the upper supply voltage source is
16	applied;

- a fourth transistor of the first conductivity type having a source node to which lower supply voltage is applied, a gate node to which an input signal is applied externally, and a drain node which is an input to the buffer output portion.
- 1 14. (New) The integrated circuit of claim 13, wherein the first and fourth
  2 transistors are NMOS transistors, and the second and third transistors are
  3 PMOS transistors.
- 1 15. (New) The integrated circuit of claim 13, wherein the large capacitor is
  2 connected between the sources of the first and fourth transistors of the
  3 buffer input portion and the gate of the second transistor of the buffer input
  4 portion.
- 1 16. (New) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to its drain.

- 1 17. (New) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to the drain of the first transistor.
- 1 18. (New) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to the gate of the third transistor.
- 1 19. (New) The integrated circuit of claim 13, wherein the buffer output portion
  2 which produces output signal comprises: a first inverter connected to the
  3 drain of the third transistor and the drain of the fourth transistor;
- 1 20. (New) The integrated circuit of claim 13, wherein the third transistor and
  2 the fourth transistor activate almost simultaneously to minimize the effects
  3 of ground noise on a delay jitter factor of said input buffer.
- 1 21. (New) The integrated circuit of claim 12, wherein the large capacitor
  2 charge couples the bias node of the input buffer receiver to the lower
  3 supply voltage of the input buffer receiver and wherein a capacitance
  4 value of the large capacitor is selected by the formula:

$$\frac{\text{CHC}}{\text{Cp+CHC}} \approx 1$$

6 where:-

7		CHC is the capacitance value of the large capacitor,
8		and
9		<b>Cp</b> is the capacitance value of the parasitic capacitor.
1	22.	(New) The integrated circuit of claim 12, wherein the capacitance value of
2		the large capacitor relative to said parasitic capacitor results in a quicker
3		response time for the output signal.
1	23.	(New) A method for minimizing effects of ground noise on an input buffer
2		receiver comprising the steps of:
3		forming a buffer input portion for receiving an input signal on a
4		substrate;
5		forming a bias node within said buffer input portion;
6		connecting said a lower supply voltage to said buffer input portion;
7		forming a large capacitor between the bias node and the lower
8		supply voltage said large capacitor providing a coupling ratio
9		between said large capacitor and a parasitic capacitor coupled
0		between said bias node and a ground reference point
1		approaching a unity value such that a biasing voltage at said
2		biasing node follows said lower supply voltage to minimize

13		effects of a ground noise signal between the lower supply
14.		voltage and the ground reference point; and
15		forming a buffer output portion on said substrate in communication
16		with the buffer input portion for producing an output signal.
1	24.	(New) The method of claim 23, wherein forming the buffer input portion
2 .		further comprises the steps of:
3		forming a first transistor of a first conductivity type on said
4		substrate;
5		applying the lower supply voltage to a source node of the first
6		transistor;
7		applying a reference voltage to a gate node of the first transistor;
8		connecting a drain node of the first transistor to develop as biasing
9		voltage at said drain node;
10		forming a second transistor of a second conductivity type on said
11		substrate;
12		connecting a drain node of the second transistor to the drain node
13		of the first transistor;

14	connecting a gate node of the second transistor to the drain node of
15	the first transistor for developing the biasing voltage; and
16	connecting a source node of the second transistor to an upper
17	supply voltage;
18	forming a third transistor of the second conductivity type on said
19	substrate;
20	connecting a drain node of the third transistor to the drain of a
21	fourth transistor;
22	connecting a gate node of the third transistor to the drain node of
23	the first transistor for developing the biasing voltage;
24	connecting a source node of the third transistor to the upper supply
25	voltage source;
26	forming a fourth transistor of the first conductivity type on said
27	substrate;
28	connecting a source node of the fourth transistor to the lower
29	supply voltage;
30	connecting a gate node of the fourth transistor to receive an input
31	signal externally; and

32		connecting a drain node of the fourth transistor to an input to the
33		buffer output portion.
1	25.	(New) The method of claim 24, wherein the first and fourth transistors are
2		NMOS transistors, and the second and third transistors are PMOS
3		transistors.
1	26.	(New) The method of claim 24, wherein forming the large capacitor
2		comprises the step of:
3		connecting said large capacitor between the sources of the first and
4		fourth transistors of the buffer input portion and the gate of the
5		second transistor of the buffer input portion.
1	27.	(New) The method of claim 24, wherein forming the buffer input portion
2		further comprises the steps of:
3		connecting the gate of the second transistor to its drain.
1	28.	(New) The method of claim 24, wherein forming the buffer input portion
2		further comprises the steps of:
3		connecting the gate of the second transistor to the gate of the third
4		transistor.

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29. (New) The method of claim 24, wherein forming the buffer output portion 1 which produces output signal comprises the step of: 2 forming a first inverter on said substrate; and 3 connecting an input of said first inverter to the drain of the third 4 transistor and the drain of the fourth transistor; 5 30. (New) The method of claim 24, wherein the third transistor and the fourth 1 2 transistor activate almost simultaneously to minimize the effects of ground noise on a delay jitter factor of said input buffer. 3 31. (New) The method of claim 23, wherein the large capacitor charge 2 couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the 3 large capacitor is selected by the formula:  $\overline{\text{Cp + CHC}} \approx 1$ 5 where: 6 CHC is the capacitance value of the large capacitor, 7 and

**Cp** is the capacitance value of the parasitic capacitor.

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1	32.	(New) The method of claim 23, wherein the capacitance value of the large
2		capacitor relative to said parasitic capacitor results in a quicker response
3		time for the output signal.

- 33. (New) An apparatus for minimizing effects of ground noise on an input buffer receiver comprising:
- means for forming a buffer input portion for receiving an input signal
  on a substrate;
- 5 means for forming a bias node within said buffer input portion;
- 6 means for connecting said a lower supply voltage to said buffer
  7 input portion;

means for forming a large capacitor between the bias node and the lower supply voltage said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point; and

16		means for forming a buffer output portion on said substrate in
17		communication with the buffer input portion for producing an
18		output signal.
1	34.	(New) The apparatus of claim 23, wherein forming the buffer input portion
2		further comprises:
3		means for forming a first transistor of a first conductivity type on
4		said substrate;
5		means for applying the lower supply voltage to a source node of the
6		first transistor;
7		means for applying a reference voltage to a gate node of the first
8		transistor;
9		means for connecting a drain node of the first transistor to develop
10		as biasing voltage at said drain node;
11		means for forming a second transistor of a second conductivity type
12		on said substrate;
13		means for connecting a drain node of the second transistor to the
14		drain node of the first transistor;

15	means for connecting a gate node of the second transistor to the
16	drain node of the first transistor for developing the biasing
17	voltage; and
18	means for connecting a source node of the second transistor to an
19	upper supply voltage;
20	means for forming a third transistor of the second conductivity type
21	on said substrate;
	manns for compositing a drain made of the third transister to the
22	means for connecting a drain node of the third transistor to the
23	drain of a fourth transistor;
24	means for connecting a gate node of the third transistor to the drain
	node of the first transistor for developing the biasing voltage;
25	node of the hist transistor for developing the biasing voltage,
26	means for connecting a source node of the third transistor to the
27	upper supply voltage source;
28	means for forming a fourth transistor of the first conductivity type on
29	said substrate;
30	means for connecting a source node of the fourth transistor to the
31	lower supply voltage;

32		means for connecting a gate node of the fourth transistor to receive
33		an input signal externally; and
34		connecting a drain node of the fourth transistor to an input to the
35		buffer output portion.
1	35.	(New) The apparatus of claim 24, wherein the first and fourth transistors
2		are NMOS transistors, and the second and third transistors are PMOS
3		transistors.
1	36.	(New) The apparatus of claim 24, wherein means for forming the large
2		capacitor comprises:
3		means for connecting said large capacitor between the sources of
4		the first and fourth transistors of the buffer input portion and the
5		gate of the second transistor of the buffer input portion.
1	37.	(New) The apparatus of claim 24, wherein means for forming the buffer
2		input portion further comprises:
3		means for connecting the gate of the second transistor to its drain.
1	38.	(New) The apparatus of claim 24, wherein means for forming the buffer
2		input portion further comprises the steps of:

- means for connecting the gate of the second transistor to the gate

  of the third transistor.
- 1 39. (New) The apparatus of claim 24, wherein means for forming the buffer output portion which produces output signal comprises:
- means for forming a first inverter on said substrate; and
- means for connecting an input of said first inverter to the drain of
  the third transistor and the drain of the fourth transistor;
- 1 40. (New) The apparatus of claim 24, wherein the third transistor and the
  2 fourth transistor activate almost simultaneously to minimize the effects of
  3 ground noise on a delay jitter factor of said input buffer.
- 1 41. (New) The apparatus of claim 23, wherein the large capacitor charge
  2 couples the bias node of the input buffer receiver to the lower supply
  3 voltage of the input buffer receiver and wherein a capacitance value of the
  4 large capacitor is selected by the formula:

$$\frac{\text{CHC}}{\text{Cp+CHC}} \approx 1$$

6 where:

7		CHC is the capacitance value of the large capacitor
8		CHC, and
9		Cp is the capacitance value of the parasitic capacitor
10		Cp.
,1	42.	(New) The apparatus of claim 23, wherein the capacitance value of the
2		large capacitor relative to said parasitic capacitor results in a quicker
3		response time for the output signal.

## **Abstract**

[0025] A particular input buffer receiver includes a buffer input portion for receiving an input signal, a large capacitor between a bias node and the lower supply voltage, and a buffer output portion for producing an output signal. The circuit works to remove ground noise by charge coupling the bias voltage developed at the bias node to the lower supply voltage of the input device.

# **Annotated Drawing Sheet(s) Showing Changes**



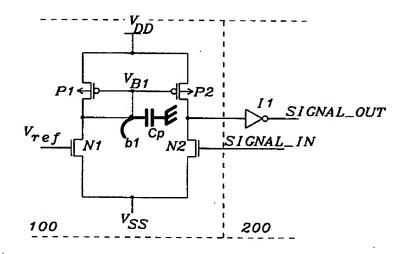


FIG. 1 - Prior Art

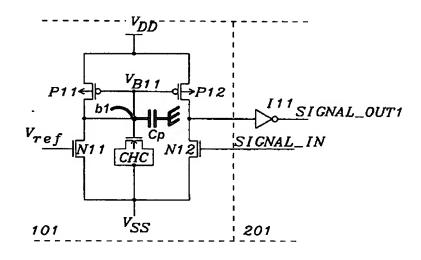


FIG. 2

Page 87 of 89

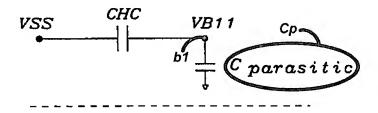


FIG. 4A

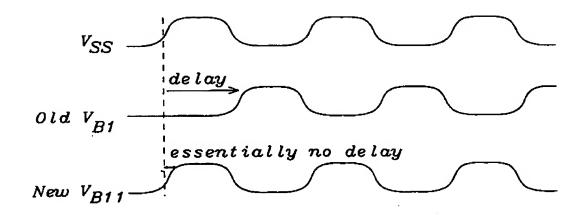


FIG. 4B

Page 88 of 89

**Drawing Replacement Drawing Sheet(s)**